International Journal of Advanced Technology & Engineering Research (IJATER)
www.ijater.com

FERROELECTRIC MEMORY

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***Abstract*—The current standing of developments within the field of ferroelectric memory devices has been considered. The rapidly growing market of non volatile memory devices has been analysed, and the current state of the art and prospects for the scaling of parameters of non volatile memory devices of different type considered. the fundamental constructive and technological solutions within the field of the look of ferroelectric letter of the memory devices, still because the " roadmaps" technology, are mentioned.This analysis paper focuses on the implementations of " Battery Less sensible phones" , and on its pros and cons. It will also state some of the economic and potential changes that may be created as per our research.**

***Keywords*—Advantages, Astonishing Technology, Battery drain, Computer Science, Disadvantages, Economy Factor, Incentives, Invention.**

I. INTRODUCTION

Extensive investigations of semiconductors and ferroelectricity had been started at about the same time—in the first postwar years. In those years, the discovery was made of barium titanate—the precursor of the largest currently available class of oxygen octahedral ferroelectrics (Wul and Goldman,1945);then, in 1947, Shockley, Bardeen, and Brattain discovered the so called transistor effect, for which, later,in 1956, all three were awarded the Nobel Prize in Physics.

By the late 1950s, the basic elements of the semiconductor technology had been developed, and Kilby and Noyce designed an integrated circuit . In 1960s,Wanlass and Sah planned the conception of complementary logic (1963), and developed the semiconductor. Since then, the main driving force behind the development of the semiconductor industry has been the constant increase within the degree of integration (the number of components on a chip), that is enforced by decreasing the minimum topological dimensions provided by means of lithography .Already in the 1950s, in parallel with the theoretical conceptualization of the physics of ferroelectric phenomena, there has begun an active search for practical applications of ferroelectrics, in particular, for the purpose of designing and fabricating memory devices.

This initial stage of these works has not been finished with significant practical results: the market has been conquered by ferromagnetic analogs .The next wave interest within the ferroelectric alphabetic memory has emerged in the 1970s along with the appearance of the thought integration ferroelectrics with the semiconductor technology.In particular,Wu proposed and element supported the semiconductor duringwhich a ferroelectric was used as the gate insulator.

Potentialof victimization ferroelectrics within the semiconductor technology has become clear about twenty years ago. This has found reflection in the emergence of a new interdisciplinary direction that combines research within the field of the technology of recent materials, the physics of ferroelectric structures, and the integration with microelectronic processes, i.e., " integrated ferroelectrics" . The attractiveness of the idea of the integration of ferroelectrics with microelectronic technologies is associated with their unique physical properties.

This makes it possible to use ferroelectric materials within the style of recent categories of devices intended for receiving, storing, and processing information (memory devices, elements with a high specific capacity for technologies of ultra large scale integration, micro electromechanical systems and sensors, electrically tunable devices operating in the microwave and optical ranges of frequencies.

II. NON VOLATILE MEMORY DEVICES AND ASPECTS

In recent years, the rapid development of mobile devices has attracted the particular attention of manufacturers to nonvolatile memory technologies. Today, in the market, there are completely different categories of storage devices, which occupy separate niches for their application. However, there is anacute need for the advent of new types of devices. The semiconductor industry has performed a search for the so called " ideal memory."

This memory should combine the speed with the non volatility of to the flash memory to its capacity.

Now a days flash memory is the leader of non volatile memory devices. The working principle behind it is the ejection of hot carriers from transistor to the on floating gate so that it imposes restrictions on number of switching systems and writing speed. But the problem comes when we want to restrict the size of the insulator and increase the charge carriers. There are some memory devices that can help you with such parameters. Among this list FRAM tops the list

MRAM uses quantum mechanical tuning of spin polarized electronics separating the layers. The layers differentiate the high or low resistance of cell. The problem is that the lateral distribution of random fields. There by the importance or having a ferroelectric memory has increased. Thus the inventions has taken place Similar problems, which are associated with the necessity of using high writing currents and,corre spondingly, large sizes of transistors providing their.

Figure i. FRAM CHIP

1. within the literature, per the semiconductor memory nomenclature, the abbreviation FRAM or FeRAM stands for ferroelectric random access memory.
2. The abbreviation MRAM stands for agnetoresistive random access memory.

The abbreviation pusher stands for action random access memory. generation, are limitations of the PRAM scaling. The cell sometimes consists of 1 semiconductor device and one resistance (1T/1R).

Programming requires sufficiently high currents for rapid heating of the chalcogenide element (According to the Joule heating, there exists a phase transition from the state to the polycrystalline state). The principles of organization of this memory type have been repeatedly demonstrated; however, the potential of the pusher scaling continues to be not clearly understood, because, with a further decrease in the dimension of the cells due to the heat dissipation will lead to a disruption of opera tion of the adjacent cells. In general, FRAM devices have a higher potential for scaling than their analogs visible of the charge principle of writing and the possibility of decreasing the layer thickness to several monolayers (see, for example,). However, the proportion of such devices in the market is still insignificant and does not meet the expectations of the industry. Pesent, the capacity of FRAM equals to only 0.0001 of the DRAM or flash memory capacity. This situation can be associated with the serious problems regarding the integration of new materials. In the integrated circuit technology, the advent of multicomponent oxides with a high crystallization temperature and a reactivity of components, which are sensitive to effects caused by many standard processes occurring in the microelectronic technology, has significantly complicated the technological process and necessitated the development of several tens of related technological operations. The technical complexity in the way of implementing new devices has been, as before, the matter that is additionally acquainted to the level opers of new materials, namely, the impossibility of using the currently available technological equipment for testing the developed processes because of the high probability of its contamination with active chemical elements of these compounds. This circumstance has required significant investments in the construction of technological pilot lines and fabs for production of microelectronic devices (for example, the Matsushita Electric Industrial Company). Finally, until recently, ferroelectric memory technology had no products that might be important for the trade by itself(“ killer application”). Once the product falls into this category, the industry concentrates enormous resources for transferrable it to needs of the market. Let us now consider the state of the art and road maps (Roadmap) of the FRAM technology (Table 1). In 2001, the semiconductor industry involved the technology for fabricating elements with a dimension of a hundred thirty nm, whereas the dimension of elements of the FRAM devices produced at that time reached 500 nm. For three years, the FRAM technology had demonstrated a very high rate of development when the general level of dimensions of technology elements reached 90 nm. In 2004, the dimension of ferroelectric elements was reduced to 180 nm. Unfortunately, what follows had been a protracted amount of stage nation, which was associated with the development of new constructions and materials. The next technological standard of the dimension of ferroelectric elements (130 nm) ought to be down by 2013, and semiconductor fabs should work with the feature size of 32 nm. Further, according to the predictions, there will be a four year cycle of development of new design rules.

The scaling of technological parameters is connected with the solution of a number of serious problems encountered in the FRAM technology. The main task for the nearest future is to improve the parameters of the ferroelectric employed in the cell style, where the ferroelectric capacitor is formed over the transistor structures and for the distant future, it is the development of three dimensional (3D) structures of the cell.

III. FRAM: DESIGN AND TECHNOLOGY

Historically, in the first version of the design of FRAS ferroelectric was used as the gate insulator (a cell consisting of only one transistor, which, according to the modern classification, is designated by 1T). A change in the state of polarization of the ferroelectric ends up in the modulation of the surface potential of the semiconductor and, correspondingly, to the gap or closing of the conducting channel of the metal– ferroelectric– semiconductor (MFS) transistor (Fig. 2). This is the best method to organize the operation of memory devices: it ensures the smallest form factor of the cell, and the reading does not require polarization switching. However, at a similar time, this variant is very difficult to realize in observe, because, within the method of high temperature deposition, the ferroelectric and silicon react with each other, which leads to the manifestation . Dynamic of uncontrollable properties of the interface (see, for example) .

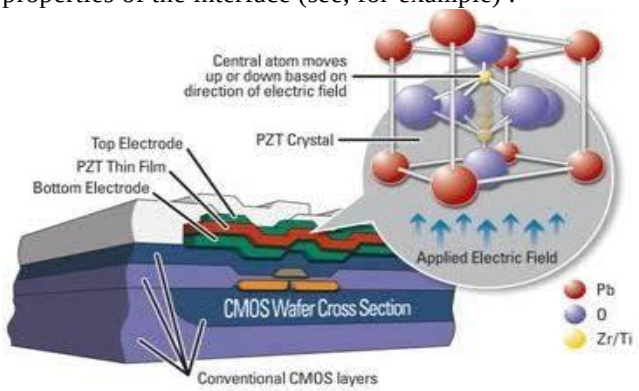

Figure ii. LAYERS OF F RAM

Research works performed in this direction are concerned with attempts to implement the direct epitaxial growth of a ferroelectric layer on semiconducting material (see, for example) or with the use of barrier layers (see, for example). Although there are some achievements during this direction, in general, it is still far short of industrial solutions. In order to prevent oxidation of silicon, some attempts have also been made to grow fluoride ferroelectrics of the BaMgF4 type. However, the solution closest to implementation is connected with the employment of terribly skinny barrier layers (with a thickness of several nanometers), such as HfO or LaAlO3 and their technology has been actively developed in business with the aim of substitution thermal oxides.

The most extensively employed now is another method for organizing cells of memory devices using ferroelectric capacitors and one or more transistors operating within the switch mode (for example, cells consisting of 1 electronic transistor and one condenser (1T/1C), as well as 2T/2C, 6T/4C, and the so called chain FRAM with the cell consisting of a chain of transistors and capacitors connected in parallel, by analogy with the concept of NAND5 flash memory address architecture) . The most important stage of the technological cycle is that the deposition of a skinny ferroelectric layer. The deposition method should guarantee a certain management of the stoichiometric ratio of components, the phase composition, and the crystal structure. Furthermore, in order to achieve a high degree of integration in the next few years, it'll be necessary to produce sensible step coverage of the relief with a high aspect ratio. For example, the chemical vapor deposition methods have often bad step coverage because of the diffusion limited mechanism of transport of the initial components (the rate is comparatively high on the surface and rather low at the lowest of the ditch owing to the difficulties encountered in the delivery of the precursors).The main deposition methods, which satisfy the requirements of the semiconductor manufacturing, are as follows: chemical solution deposition (CSD), physical vapor deposition (PVD), chemical vapor deposition (CVD), misted source chemical solution deposition (MSCSD), and atomic layer deposition (ALD). Comparative characteristics of the methods used for deposition of ferroelectric layers are presented in.

IV. NAND AND NOR REPRESENT TOTALLY DIFFERENT PRINCIPLES OF NON-VOLATILE STORAGE

1. Organization: The NAND style of alphabetic characterory non-volatile storage{nonvolatile storage} combines memory cells into AN array, that ensures a high degree of interconnection between the cells, in contrast to the NOR type of flash memory, that permits true random access to every individual cell. The NOR sort operates sort of a memory device, whereas the NAND type operates like a hard disk drive. The problems regarding the control of the stoichiometric composition have been successfully solved using the methods of chemical deposition from solutions (sol– gel method) and misted source chemical solution deposition. However, the classical sol– gel method (spinon technique) forms a planar surface, whereas its modification, i.e., misted source chemical solution deposition, provides a good step coverage on submicron reliefs. An even more promising technique for the deposition on complex topographic reliefs is the atomic layer deposition method, which has been intensively developed for the deposition of multicomponent oxides.

The sequence of technological operations in the fabrication of FRAM devices makes it potential to use the standard CMOS process. First, there occurs a conventional high temperature process of fabricating transistor structures (the so called “ frontend” process), which is completed by the process of melting of borophosphosilicate glass (BPSG). Then, there comes the FRAM cycle of fabricating the ferroelectric capacitor, followed by the standard low temperature

" back end" process of inter level metallization. Let us consider examples of implementation of the FRAM technology. The FRAM (64 Mbit) developments made by the Texas Instruments Company in cooperation with the well known Ramtron Corporation have used a stacked structure of the ferroelectric capacitor formed over the transistor elements using an inter level tungsten contact (Wplug). Tungsten is very susceptible to oxidation; hence, it is covered by the TiNAl barrier layer. It also serves as an adhesion layer for the subsequent iridium layer, which prevents oxidation of titanium. This is followed by the atomic number 77 chemical compound layer, which is in contact with the layer of lead zirconate titanate (PZT). A similar system of electrodes layer is adjacent to the noble metal layer, that exerts associate degree orienting effect. The Matsushita Electric Industrial Company has developed the process of integration of SrBi2(TaxNb1 – x)2O9 (SBTN), which is a material that, as is understood, doesn't exhibit a fatigue impact, but requires a higher crystallization temperature [28]. A similar combination of layers has been used as electrodes: Wplug– TiN– Ir– IrO2– Pt. A direct contact with the ferroelectric layer is provided by a 100nm thick noble metal layer, which, as in the case of PZT, exerts associate degree familiarizing impact within the formation of the SBTN crystal structure. From the bottom and from the top, the capacitance is protected by a barrier layer in order to prevent degradation of the ferroelectric during the subsequent technological operations in a hydrogen containing atmosphere. Unlike the majority of manufacturers, the Toshiba Company has used a sequence design within which the cell consists of a electronic transistor and a ferroelectric capacitor connected in parallel. For purposes to increase the capacity, two capacitors fabricated in the form of a triangle square measure settled on one bottom electrode. At present, it's the quickest memory with the low est power consumption. The achieved characteristics have opened up new important potential markets for this branch of the trade (this product has within the list of the most promising achievements of the " killer application" industry). In particular, it has been reported that these structures may be used because the cache memory for solid state and magnetic storage devices, which makes it attainable to extend the speed of professional gram execution by a factor of 1.5. In Russia, the first samples of FRAM were fabricated in the early 1990s (the joint developments of the JSC " Mikron" and MIREA). A 6T/2C cell and a 3µm method were used for fabricating the capacitors formed by the sol– gel method in combination with a unique electrochemical method of synthesizing the initial solutions. However, the developed FRAM samples have not gone into mass production due to the change of the situation in the country. At present, interest has been again expressed by integrated circuit manufacturers in the FRAM technology due to the reconstruction of domestic plants for the production of microelectronics. The joint development of the JSC " Angstrem" and MIREA has used the " silicononsapphire" process, so that it has become possible to retain the sufficiently high performance characteristics of the PZT layer (polarization, 40 µC/cm2; coercive voltage, 1 V).

V. CONCLUSIONS IN THE FRAM MARKET, THERE HAD BEEN A SUFFICIENTLY

Long period, during which this branch of industry could not overcome the barrier of a hundred and eighty nm for the minimum size of the ferroelectric element, which was connected with the integration of new materials into the semiconductor technology. In recent years, it has become possible to achieve extremely high perfor. Comparatmance characteristics of FRAM devices with low power consumption. This has opened up prospects for their wide application in mobile devices. At present and in the nearest future, stacked type structures will be used with a gradual transition to three dimensional elements. Ferroelectric films, as before, will be produced using the chemical solution deposition (CSD) and chemical vapor deposition (CVD) methods. However, the reduction in the size of the FRAM elements will necessitate the use of methods that make sure the best conformity of the relief reproduction, such as the misted source chemical solution deposition (MSCSD) and atomic layer deposition (ALD) methods. A further reduction in the size and thickness of the ferroelectric part can cause the necessity of mistreatment the direct epitaxial growth of ferroelectric perovskites on silicon and designing transistor structures with a gate ferroelectric.

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