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SELECTIVE HARMONIC COMPENSATED SERIES SQUARE WAVE INVERTERS

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Abstract:

The quest for achieving Freedom of control, efficient conversion and reliability drove the power technology increasingly towards the use of power electronic devices in recent decades. These devices however introduce undesirable harmonics into the interconnected systems, which triggers mal-operation and reduces the lifetime of connected systems. Several efforts have been done towards the mitigation of these inherent harmonics of power electronic switching systems in the areas of control, topology, auxiliary circuitries and system placement. This paper presents a low-frequency square-wave inverter, with a series-connected pulse width modulated (PWM) inverter. The series compensators produce only the desired harmonic voltages to make the net output voltage sinusoidal with small PWM switching harmonics. No external dc source or active power at fundamental frequency is required to control the dc bus voltage of these additional series cells. Theoretical analysis of this strategy is presented in this paper with simulation and experimental results.

***Index Terms*—Square wave inverter, power converters, PWM, SHE PWM, Series compensation, Power quality, Harmonic Mitigation.**

I. INTRODUCTION

Power electronic equipment application and usage has recently seen tremendous growth in industry and utility networks. With this has grown the urge for novel power converters having best possible reliability with least possible cost. Multilevel inverters have emerged as one such equipment in medium and high voltage applications. They comprise of an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped high voltage waveforms at the output, with power semiconductors being exposed to reduced voltages.

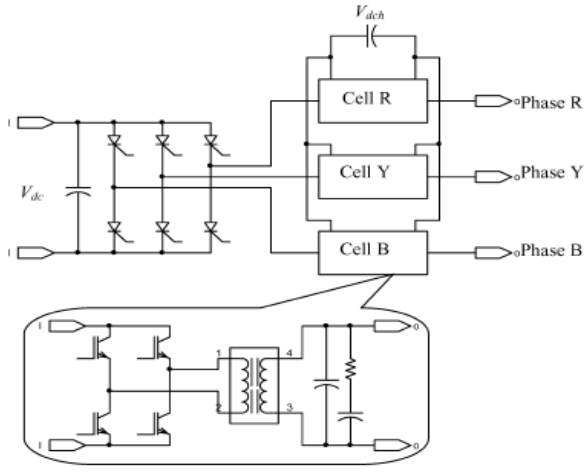


Figure 1: Basic converter topology

If *m* is the number of steps of the phase voltage with respect to the common terminal, then the number of steps in the line voltages between two phases of the load and the number of steps ***p*** in the phase voltage of a three-phase star connected load are *k=2m+1* and *p=2k-1* respectively.

Three topologies are popular in case of multilevel inverters namely diode-clamped (neutral-clamped) [2]; capacitor-clamped (flying capacitors) [3] and cascaded multicell inverters [1].

Demands suiting medium-voltage high-power inverters has made cascade inverter to be extensively used in high-power medium voltage applications such as conveyors, mills, blowers, compressors, and pumps etc. This paper emphasises on a cascaded multilevel inverter and presents a comprehensive analysis of selective harmonic elimination scheme for a MLI for minimisation of harmonics and optimised voltage outputs.

II. SELECTIVE HARMONIC ELIMINATION

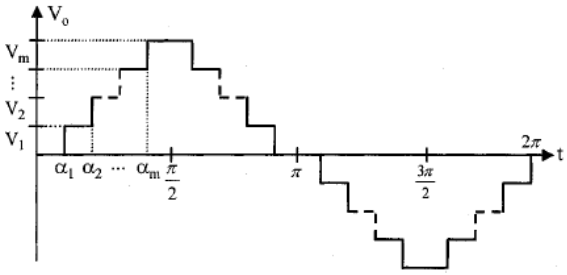


Figure 2: Stepped voltage waveform.

A stepped voltage waveform synthesized by a (2m+1) level inverter is shown in figure 2, where m is number of switching angle instants. Application of Fourier analysis provides the amplitude of odd nth harmonic of the stepped waveform as [4] with amplitude of all even harmonics as zero

$$h_n = \frac{4}{n\pi}\sum_{k=1}^{m}[V_k \cos(n\alpha_k)] \quad \text{.....(1)}$$

Where Vk is the kth level of dc voltage, n is an odd harmonic order, m is the number of switching angles and αk is the kth switching angle. According [19] α1 to αk must satisfy α1< α2<.....< αk<π/2. To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to (m-1) harmonic contents can be eliminated from the voltage waveform. The most significant low-frequency harmonics are selected for elimination, by proper selection of angles among different inverters. For the number of eliminated harmonics at a constant level, all switching angles must be less than π/2.

This modulation strategy has a drawback that it provides a narrow range of modulation index.

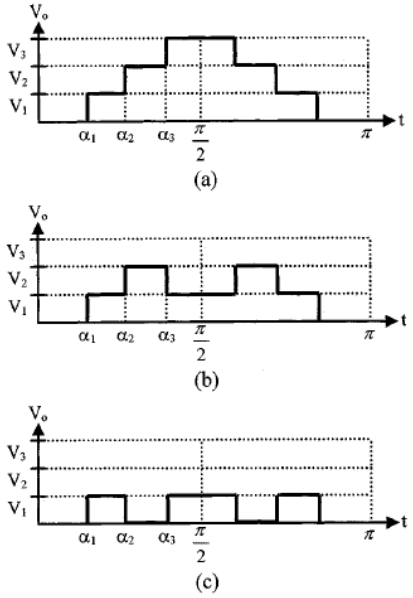


Figure 3: Seven-level stepped waveform half-cycle for modulation index ranges. (a) High modulation index. (b) Intermediate modulation index. (c) Low modulation index.

In order to achieve a wide range of modulation indexes with minimized THD, a generalized selected harmonic modulation scheme was proposed [8]. The method can be illustrated by figure 3 showing the positive half-cycle of seven-level stepped waveforms for various modulation index levels. The range of modulation indices is hown to be divided into three levels high, middle, and low. An output waveform with a high modulation index level when α3 > π/2, shown in figure 3(a) no longer exists and thus an output waveform shown in figure 3(b) for middle modulation index level is applied. And when the switching angles α1 to α3dont converge at a low modulation index, the output waveform in figure 3(c) can be used. Thus a stepped waveform comprising of m switching angles can be divided into m modulation index levels. With this approach low switching frequencies with minimized harmonics in the output waveforms can be achieved for wide range modulation indexes.

The harmonic elimination technique is very suitable for inverters control. By employing this technique, the low THD output waveform can be obtained without using any filter circuit. The switching devices too, turn on and turn off only once per cycle. In the three-phase inverter, the aim is to use this switching scheme to achieve the fundamental voltage and eliminate the fifth, seventh and 11th harmonics, etc (n = 1, 5, 7, 11, 13, 17, 19, "). A generalized harmonic expression for multilevel stepped voltage has been derived [9] and is expressed as where positive sign represents the rising edge, and the negative sign represents a the falling edge.

$$h_n = \frac{4}{n\pi} \times [V_1 \cos(n\alpha_1) + V_2 \cos(n\alpha_2) \pm \cdots . \pm V_m \cos(n\alpha_m)]$$

.....(2)

The SHE has been an attractive alternative to traditional pulse-width modulation technique. In this method there is no need to calculate the firing angles for placing notches. Here, the lower order harmonics are attenuated by the dominant harmonics of same order of opposite phase by sinusidal PWM inverter. This is achieved by varying the phase angle of the carrier wave of the sinusoidal Pulse Width Modulation (PWM) inverter [5], which generates dominant harmonics with bands close to the amplitude of dominant voltage harmonics present in the system though having opposite polarity. In this method the Total Harmonic Distortion (THD) for 3rd, 5th, 7th and 9th order harmonics is determined followed by calculation of harmonics amplitude for these with help of Total Harmonic Distortion (THD). After calculating amplitude, injecting the same order of harmonics in opposite amplitude Thus the resultant disorder sine wave is compared with triangular waveform and results in pulse are produced and will give to the switches. This method is simple and easy implementation method for reducing the Total Harmonic Distortion (THD).

III. SELECTIVE HARMONIC COMPENSATED SERIES INVERTER

Selective harmonic compensated MLI has series-connected single-phase PWM inverter that produces the required harmonic voltages in addition to the three phase fundamental voltage component. These three single-phase cells normally have common dc bus voltage. Usually, the value of this common dc bus voltage is less than that of the main square-wave inverter. The present work uses natural open-loop without drawing any active power at fundamental frequency. The square-wave voltage varies from $+V_{dc}/2$ to $-V_{dc}/2$, with the time period of $2\pi/\omega_f$. Mathematically, it can be expressed using the unit step function $u(t)$ as follows:

$$V_S(t) = \sum \left[V_{dc} \left\{ u\left(t - 2n\frac{\pi}{\omega_f}\right) - u\left(t - (2n+1)\frac{\pi}{\omega_f}\right) \right\} \right] - \frac{V_{dc}}{2}, \qquad n = 0, \pm 1, \pm 2, \pm 3$$

.....(3)

The active power drawn at harmonic frequencies regulates the dc bus voltage of the series compensator. The desired series compensator output voltage can now be obtained as

$$V_h(t) = \sum_{n=3}^{\infty} \left[\frac{4\,(V_{dc}/2)}{n\pi} \sin(n\omega_f t) \right]$$

.....(4)

Where n is odd, and for a perfect compensation the DC link voltage becomes,

$$V_{load}(t) = \frac{4\,(V_{dc}/2)}{\pi} \sin(\omega_f t)$$

.....(5)

If the modulation depth (m) of the nth harmonic component of the series compensator is assumed as 4/nπ, the output nth harmonic component of the series compensator is given as;

$$V_{nh}(t) = mV_{dch}(t) \sin(n\omega_f t) = \frac{4V_{dch}(t)}{n\pi} \sin(n\omega_f t).$$

.....(6)

Where, $V_{dch}(t)$ is dc bus voltage of the series compensator at any time *t*.

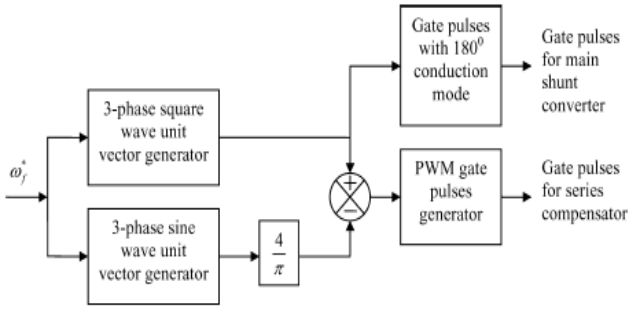


Fig. 4. Basic gate pulse generation scheme

In steady state, $V_{dch} = V_{dc}/2$ and the load voltage V_{load} becomes sinusoidal [(3)]. The fundamental load current does not affect this dc bus voltage balance as no fundamental component of voltage is present at the output of the series compensator. The block diagram of the basic switching control strategy for this topology is presented in Fig. 4.

Single-phase transformers introduce losses and also increase the cost of the system. While the transformer-less counterpart shown in Fig. 5 with the exception that the power absorbed by each compensator is $\sum_{n=5}^{\infty} P_{nh}$. The dynamical equation of the dc bus of each compensator is

$$\frac{dV_{\mathrm{dch}}(t)}{dt} = \left(\frac{V_{\mathrm{dc}}}{2} - V_{\mathrm{dch}}(t)\right) \times \sum_{n=5}^{\infty}\left[\frac{R_L}{2C_h}\left(\frac{4}{n\pi}\right)^2 \frac{1}{R_L^2 + (n\omega_f L_L)^2}\right] \quad \text{....(7)}$$

In steady state all three independent dc buses are $V_{dc}/2$, load voltage becomes sinusoidal with small switching harmonics of series compensator.

In this topology, several single-phase full-bridge inverter cells are connected in series similar to multicell topologies [3]. Each cell handles only one harmonic component and is named as *n*th harmonic cell (Fig. 6). Modulation depth "*m*" is taken as 1 for all the cells. Equation (5) is now modified for the *n*th harmonic voltage at the output of the *n*th cell is as

$V_{nh}(t) = mV_{\mathrm{dch}}(t)\sin(n\omega_f t) = V_{\mathrm{dch}}(t)\sin(n\omega_f t)$

The average power of the *n*th harmonic cell is then

$$P_{nh} = \frac{1}{2}\frac{((4/n\pi)(V_{\mathrm{dc}}/2) - V_{\mathrm{dch}}(t))}{R_L^2 + (n\omega_f L_L)^2} V_{\mathrm{dch}}(t)\, R_L \quad \text{....(8)}$$

Using power balance as before, the dynamics of the *n*th cell dc bus becomes

$$\frac{dV_{\mathrm{dch}}(t)}{dt} = \left(\frac{2V_{\mathrm{dc}}}{n\pi} - V_{\mathrm{dch}}(t)\right)\left[\frac{R_L}{2C_h}\frac{1}{R_L^2 + (n\omega_f L_L)^2}\right] \quad \text{.....(9)}$$

In steady state, the dc bus voltage of the *n*th harmonic cell becomes $2V_{dc}/n\pi$. Thus dc bus voltage of each cell differs from other cell. The higher harmonics will require lower dc bus voltages.

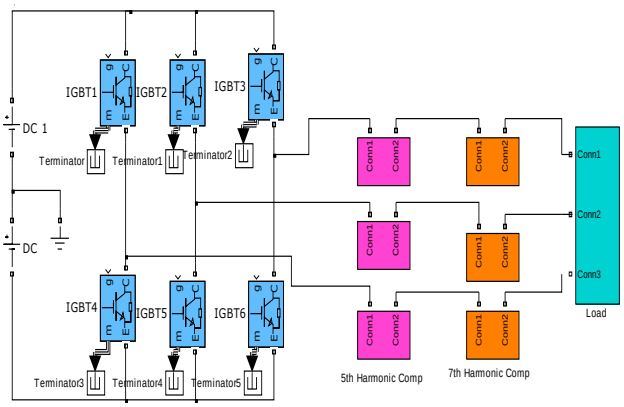


Fig. 5. Topology for SHE MLI.

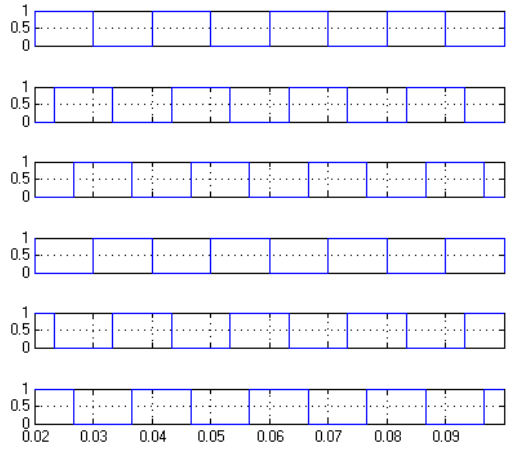
IV. SIMULATION SETUP

The schemes elaborated in section II & III are implemented in Matlab Simulink environment using IGBT's and the switching pulses are produced by soft switching technique for fundamental three phased full bridge and for series connected compensator cell H bridges.. The dominant 5th and & 7th harmonics are targeted for mitigation as they constitute bulk of distortion.

The configuration of the simulink model is run for ODE 45 solver for a resistive load though the applicability of the presented inverter has also neen tested for reactive loads. The full bridge is fed with two isolated DC sources to produce three level square wave output voltages with a peak value of 415 volts to produce an output alteration at 50Hz.

V. SIMULATION RESULTS

The developed model for Selective harmonic compensated MLI (SHCMLI) is simulated to validate the performances on SIMULINK platform. The fixed dc bus voltage of the square-wave inverter is 415V. It operates in 180◦ conduction mode at fundamental frequency. This converter is connected to a three-phase load.



(a)

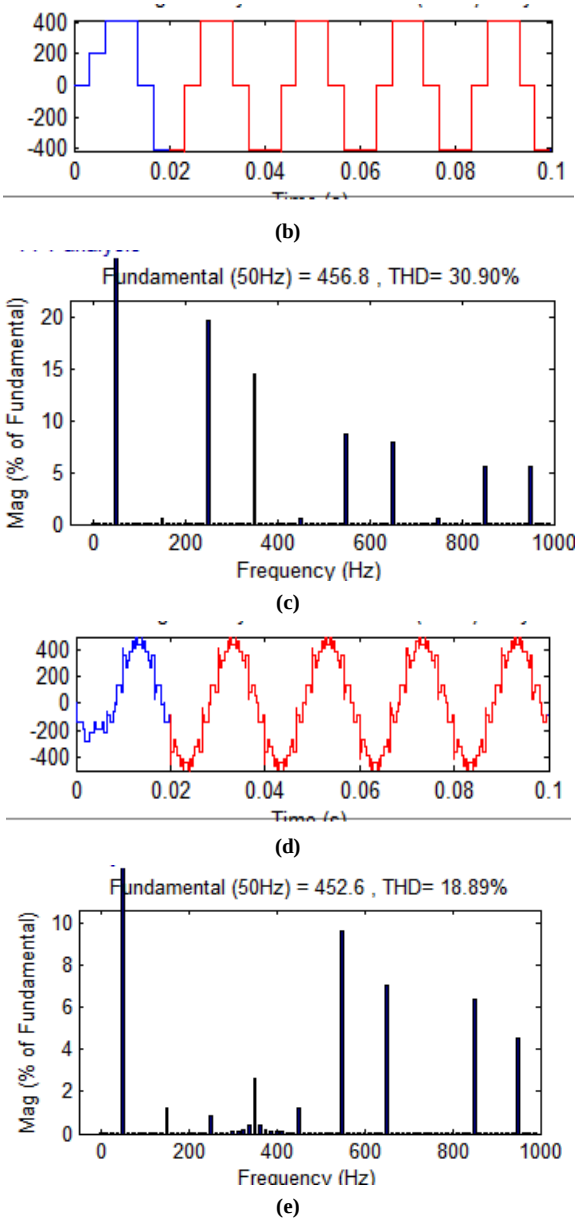


Figure 6: Simulation results (a) Switching pattern (b) Fundamental switching voltage outputs (c) Fundamental switching Harmonic Spectrum (d) SHC MLI switching voltage outputs (e) SHC MLI Harmonic Spectrum

This load consists of a voltage source of 415 V *L–L* and has series impedance. The obtained results providing switching sequence, fundamental voltage waveform and SHC MLI output voltage with its harmonic spectrum are displayed below in figure. Visual inspection of the waveforms and their spectrum themselves suggest that the lower order harmonics are significantly eliminated by the adopted technique and the waveform approach a more sinusoidal waveform.

V. CONCLUSION

An open-loop natural control scheme of voltage source inverter has been analysed through simulink platform. The main square-wave inverter is built with high-voltage low switching-frequency semiconductor devices like integrated gate commutated thyristors (IGCTs). The series compensators produce only the desired harmonic voltages to make the net output voltage sinusoidal. For medium-voltage application, several compensating PWM inverters are connected in series. Each cell compensates one particular harmonic only. As the order of harmonics increases, the required dc bus voltage level drops. It has been concluded that the dc bus of the compensators do not require any external dc source or closed-loop controller for this proposed strategy. For variable-speed drives applications, the magnitude of the fundamental output voltage should be controlled by regulating the dc bus voltage of the square-wave inverter.

The scheme studied and validated is shown in figure 7, the simulation setup provided a THD's for square wave output and SHE compensated inverters, which are shown in table 2 below. The results suggest that the dominant lower order odd harmonics i.e. 5^{th} and 7^{th} are considerably reduced and the output voltage is suitably smoothened owing to this. The residual ripples in the output waveforms can easily be filtered out for a reactive load without the requirement of any filtering device. Which is one of the most prominent advantage of this scheme.

Table 2: Comparison of SHE MLI harmonic spectrum

	Fundamental	**5^{th} Harmonic**	**7^{th} Harmonic**
Square Wave	**100%**	**20.7%**	**13.73%**
SHE Technique	**100%**	**0.82%**	**2.59%**

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