International Journal of Advanced Technology & Engineering Research (IJATER)
www.ijater.com

TIME DOMAIN ANALYSIS OF LOSSY TRANSMISSION LINES USING FDTD TECHNIQUE

Mouloud Satar[1,2], Hassan Belahrach[1,2], Abdelilah Ghammaz[2]
[1] Electrical Engineering Department, Royale Air Academic, 40000 Marrakech, Morroco
[2] Electrical systems and Telecommunications Laboratory (LSET) FSTG - University Cadi Ayyad, 40000 Marrakech, Morroco

Abstract

With the rapid evolution of VLSI technology, minimum feature size and the distance between interconnections continue to decrease. Thus transmission line effect such as crosstalk plays an important role in determining system performance.

A transient analysis of CMOS logic gates driving coupled RLC transmission lines is presented in this paper for both 90 and 65 nanometer technologies. A linear resistor model is used to approximate the CMOS driver stage and the CMOS receiver is modeled as a parallel RC loads. The lossy transmission line is analyzed in the time domain using Finite-Difference Time-Domain (FDTD) method. Some results are discussed to give insight into the crosstalk and propagations delay problems in VLSI circuits. The FDTD algorithm discussed in this study is implemented using the MATLAB programming language. To validate the FDTD computed results, PSPICE simulations are run and results are compared.

Keywords : FDTD, CMOS submicron interconnects, Crosstalk noise, Propagation delay, PSPICE, Matlab.

Introduction

Modeling and simulation of multi-conductor interconnect is of great importance in the design of high-speed integrated circuits. Recent advances in VLSI technology have brought with their requirements for high performance and high density circuits boards [1][2]. With the rapid evolution of VLSI technology, minimum feature size and the distance between interconnections continue to decrease. Thus transmission line effect such as crosstalk plays an important role in determining system performance [3]. A lossless model is not appropriate for interconnect in VLSI circuits since the parasitic interconnect resistance cannot be neglected. Also, crosstalk effects in voltage response are due to mutual capacitance and inductance between adjacent lines. Inductance effects in on-chip interconnect structure have become increasingly significant due to longer metal interconnects, reduction in wire resistance and higher clock frequencies [4]. In this paper, an efficient numerical method for transient analysis of lossy uniform transmission lines is presented. The lossy transmission line is analyzed in the time domain using Finite-Difference Time-Domain (FDTD) method. The FDTD technique is used because this method discretizes the telegrapher's equations both in time and space and the resulting difference equations are solved using the leap-frog scheme. The objective is to evaluate the peak value of the noise injected on signal when its neighboring signals make their transitions. The case of three RLC lines with inverters as drivers and loads is addressed. The change in crosstalk when the input rise time varies from 40 ps to 120 ps is presented. Some results are presented to give insight into the crosstalk problems in fast digitals circuits. Various geometrical structures can be simulated by using the per-unit-length parameter matrices R, C, L and G as primary parameters. The FDTD results were compared to the results from PSPICE simulations and good agreement has been achieved.

The FDTD solution of the multiconductor transmission lines (MTL) equations

The FDTD technique is one of the best methods which can be used to find the solution of the MTL equations [5]. This method gives accurate results and carries time domain analysis of coupled lines [6]. Consider N-coupled transmission lines represented by the telegrapher equations as :

$$\frac{\partial}{\partial x}\mathbf{I}(x,t) + \mathbf{G}(x)\mathbf{V}(x,t) + \mathbf{C}(x)\frac{\partial}{\partial t}\mathbf{V}(x,t) = 0 \quad (1)$$

$$\frac{\partial}{\partial x}\mathbf{V}(x,t) + \mathbf{R}(x)\mathbf{I}(x,t) + \mathbf{L}(x)\frac{\partial}{\partial t}\mathbf{I}(x,t) = 0 \quad (2)$$

Where :

$I(x,t)=[I_1(x,t), I_2(x,t),\ldots\ldots I_{N+1}(x,t)]^T$

$V(x,t)=[V_1(x,t), V_2(x,t),\ldots\ldots V_N(x,t)]^T$

Here :

V(x,t) and I(x,t) are the space and time-dependent voltage and current, respectively. R(x), L(x), C(x), and G(x) are per-unit-length parasitic matrices of the coupled transmission lines.

To apply the FDTD method, each transmission line under consideration is discretized into N segments each of Δx, called a spacial cell [7]. Similarly the total solution time is discretized into M sections each of duration Δt, called a temporal cell [7]. In order to provide the accuracy of the

discretization the N+1voltage points (V_1, V_2,…, V_{N+1}) are interlaced one half cell apart with N current points (I_1, I_2,…, I_N), both in space and time.

Approximating the derivatives of equations (1) and (2) using the central method, the recursive equations of voltage and current are obtained as:

$$\frac{\mathbf{I}_{i+\frac{1}{2}}^{n}-\mathbf{I}_{i-\frac{1}{2}}^{n}}{\Delta x}+\mathbf{G}\frac{\mathbf{V}_{i}^{n+\frac{1}{2}}+\mathbf{V}_{i}^{n-\frac{1}{2}}}{2}+\mathbf{C}\frac{\mathbf{V}_{i}^{n+\frac{1}{2}}-\mathbf{V}_{i}^{n-\frac{1}{2}}}{\Delta t}=0 \quad (3)$$

$$\frac{\mathbf{V}_{i+1}^{n+\frac{1}{2}}-\mathbf{V}_{i}^{n+\frac{1}{2}}}{\Delta x}+\mathbf{R}\frac{\mathbf{I}_{i+\frac{1}{2}}^{n+1}+\mathbf{I}_{i+\frac{1}{2}}^{n}}{2}+\mathbf{L}\frac{\mathbf{I}_{i+\frac{1}{2}}^{n+1}-\mathbf{I}_{i+\frac{1}{2}}^{n}}{\Delta t}=0 \quad (4)$$

The recursive equations (3) and (4) can be written as:

$$\mathbf{V}_{i}^{n+\frac{1}{2}}=\mathbf{A}_{1}^{-1}\left[\mathbf{A}_{2}\mathbf{V}_{i}^{n-\frac{1}{2}}+\mathbf{I}_{i-\frac{1}{2}}^{n}-\mathbf{I}_{i+\frac{1}{2}}^{n}\right] \quad (5)$$

$$\mathbf{I}_{i+\frac{1}{2}}^{n+1}=\mathbf{A}_{3}^{-1}\left[\mathbf{A}_{4}\mathbf{I}_{i+\frac{1}{2}}^{n}+\mathbf{V}_{i}^{n+\frac{1}{2}}-\mathbf{V}_{i+1}^{n+\frac{1}{2}}\right] \quad (6)$$

With:

$$\mathbf{A}_1=\frac{\Delta x}{2}\mathbf{G}+\frac{\Delta x}{\Delta t}\mathbf{C}\ ;\ \mathbf{A}_2=\frac{\Delta x}{\Delta t}\mathbf{C}-\frac{\Delta x}{2}\mathbf{G};$$

$$\mathbf{A}_3=\frac{\Delta x}{2}\mathbf{R}+\frac{\Delta x}{\Delta t}\mathbf{L}\ ;\ \mathbf{A}_4=\frac{\Delta x}{\Delta t}\mathbf{L}-\frac{\Delta x}{2}\mathbf{R}.$$

Boundary conditions

Assuming that the CMOS driver is replaced by a linear resistor model to drive each interconnect line in coupled structure and let source voltage Vs be a Nx1 source matrix. In this case the circuit model is given in figure 1.

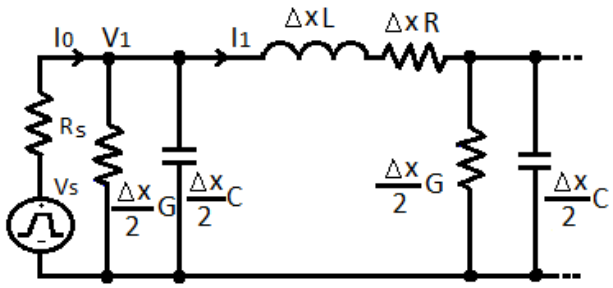

Figure 1: The circuit model at the first node

Where **Rs** represent the internal source voltage resistor.

By applying the boundary conditions at the source, the recursive equation of V1 can be written as:

$$\mathbf{V}_{1}^{n+\frac{1}{2}}=\mathbf{B}_{1}^{-1}\mathbf{B}_{2}\mathbf{V}_{1}^{n-\frac{1}{2}}+\mathbf{B}_{1}^{-1}\left[\mathbf{V}_{s}^{n+\frac{1}{2}}+\mathbf{V}_{s}^{n-\frac{1}{2}}-\mathbf{R}_{s}\left(\mathbf{I}_{1}^{n+\frac{1}{2}}+\mathbf{I}_{1}^{n-\frac{1}{2}}\right)\right] \quad (7)$$

Where :

$$\mathbf{B}_1=\mathbf{U}+\frac{\Delta x}{\Delta t}\mathbf{R}_s\mathbf{C}+\frac{\Delta x}{2}\mathbf{R}_s\mathbf{G}$$

$$\mathbf{B}_2=\frac{\Delta x}{\Delta t}\mathbf{R}_s\mathbf{C}-\mathbf{U}-\frac{\Delta x}{2}\mathbf{R}_s\mathbf{G}$$

U is the identity matrix.

Now consider that each interconnect line is terminated by a parallel R_L C_L load eventually with source voltage V_L. Applying the boundary condition at the load point, the load model at the last node is presented in figure 2.

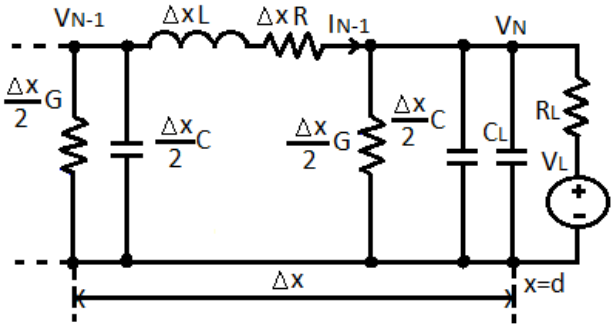

Figure 2 : The load model at the last node

The recursive equation of load voltage is obtained as :

$$\mathbf{V}_{N}^{n+\frac{1}{2}}=-\mathbf{B}_{3}^{-1}\mathbf{B}_{4}\mathbf{V}_{N}^{n-\frac{1}{2}}+\mathbf{B}_{3}^{-1}\left[\mathbf{V}_{L}^{n+\frac{1}{2}}+\mathbf{V}_{L}^{n-\frac{1}{2}}+\mathbf{R}_{L}\left(\mathbf{I}_{N-1}^{n+\frac{1}{2}}+\mathbf{I}_{N-1}^{n-\frac{1}{2}}\right)\right] \quad (8)$$

With :

$$\mathbf{B}_3=\mathbf{U}+\frac{\Delta x}{2}\mathbf{R}_L\mathbf{G}+2\frac{\mathbf{R}_L}{\Delta t}\left(\mathbf{C}_L+\frac{\Delta x}{2}\mathbf{C}\right)$$

$$\mathbf{B}_4=\mathbf{U}+\frac{\Delta x}{2}\mathbf{R}_L\mathbf{G}-2\frac{\mathbf{R}_L}{\Delta t}\left(\mathbf{C}_L+\frac{\Delta x}{2}\mathbf{C}\right)$$

Coupling noise estimation of deep submicron coupled interconnects

Crosstalk occurs mainly due to the capacitance and inductive coupling between adjacent nets [8]. Let us consider the general configuration of three RLC coupled interconnect lines controlled and loaded by inverters as illustrated in figure 3. The objective of this study is to evaluate the peak value of the noise at the far end of the victim line (node A in figure 3) for both 90 and 65 nanometer technologies.

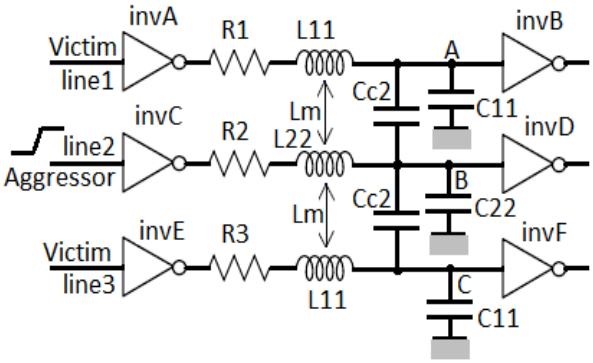

Figure 3 : Circuit schematic of three CMOS submicron interconnects.

The FDTD algorithm is implemented using the MATLAB programming language. The voltage and current are solved using Equations (5) and (6). For analysis, 20 spatial discretizations are taken for the length under consideration. The time step (Δt) is obtained as 0.0645 ps with the line velocity of 3 x 108 m/s. The FDTD results were compared to the results from PSPICE simulations. All interconnect parameters are included in table 1.

The peak value of crosstalk noise is a function of the coupled line length. A ramp signal with amplitude of Vdd and rise time of 50ps is applied to the active line. A linear resistor model is used to approximate the CMOS driver stage and the CMOS receiver is modeled as a parallel RC loads.

Table 1. Interconnect parameters per unit length for 90nm and 65nm submicron technologies [9].

Pararameters	tech 65 nm	tech 90 nm
R (KΩ/m)	449	244
C_1=C_3 (pF/m)	84.45	79.2
C_2 (pF/m)	142	132.8
C_c (pF/m)	57.65	53.62
L_{11}=L_{33} (uH/m)	1.6	1.56
L_{22} (uH/m)	1.6	1.56
L_{12}=L_{32} (uH/m)	1.43	1.38
L_{13} (uH/m)	1.3	1.22

Figure 4 shows the wave form of the crosstalk at the far end of the victim line1 (using the FDTD technique and PSPICE simulation). The case of 65nm technology is presented and the coupled length line is 1mm.

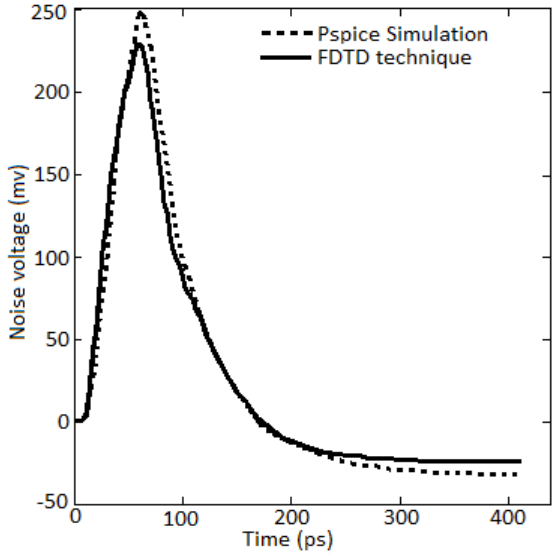

Figure 4 : Crosstalk noise wave forms at the far end of the victim line1.

The simulation results as a function of wire length for both 90nm and 65nm technology generations are plotted in figure 5.

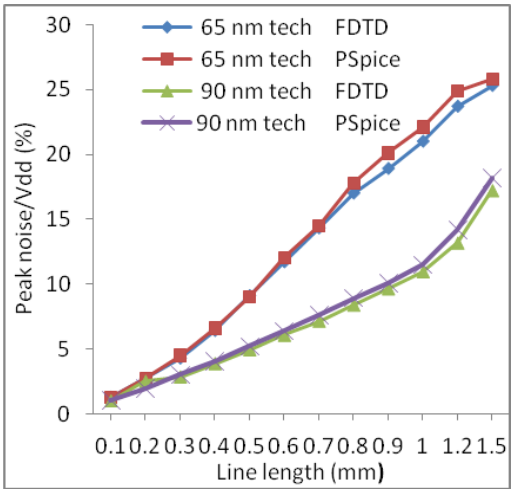

Figure 5 : Maximum crosstalk peak noise evaluation as a function of wire length.

Examining those plots, one can note that the crosstalk between parallel RLC interconnect lines increases as the interconnect length increases and as the CMOS technology scaled down into submicron region.

Delay time estimation as a function of wire length

The chosen structure is the same as that presented in figure 3. In this simulation we evaluate the impact of the coupling noise on the propagation delay Td of a CMOS inverters.

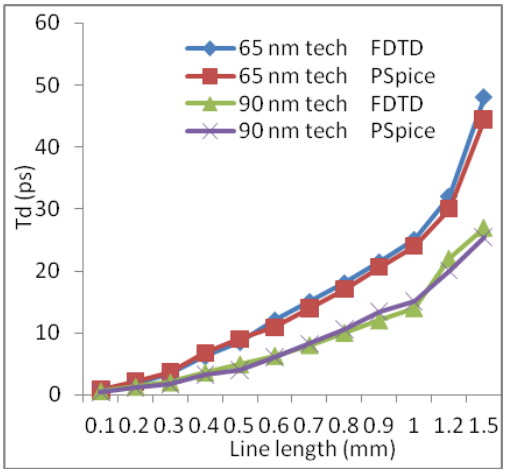

Figure 6 : Delay time estimation as a function of wire length.

The propagation delay is defined here as the time from 50% Vdd of the input to 50% Vdd of the output [10]. It is assumed that the inverter input transition is from low to high with rise/fall time of 50ps. The FDTD and PSPICE simulations results as a function of wire length for various technology generations are plotted in figure 6. Td is the propagation delay time observed at the far end of the active line (node B).

Impact of rise time on peak crosstalk noise and the propagation delay

The lines configuration is the same as that shown in figure 3. Each interconnect line is 1mm long and terminated by parallel RC loads of 50kΩ and 30fF respectively. The input aggressor rise time varies from 40ps to 120ps and all geometrical parameters are fixed.

A. Impact of rise time on peak crosstalk noise

The noise susceptibility of logic gates depends not only on the peak amplitude of the crosstalk noise, but also on its duration [11]. Figure 7 shows the change in the peak crosstalk noise at the far-end of the victim line1. The percentage error for FDTD computed peak crosstalk noise with respect to PSPICE noise is listed in Table 2 and Table 3.

Table 2 : Comparison of the crosstalk noise computed by PSPICE and our FDTD model (65 nm technology)

Rise Time (Ps)	65nm tech Vnoise/Vdd(%)	65nm tech Vnoise/dd(%)	
	FDTD	PSPICE	%Error
40	23,3	24,7	6
50	21	22,1	5,23
60	18,81	20,1	6,85
70	17,2	18,2	5,81
80	15,51	16,7	7,67
90	14,72	15,14	2,85
100	13,68	14,23	4,02
110	12,67	12,1	-4,5
120	11,8	12,2	3,38
% Average error			4.14

Table 3 : Comparison of the crosstalk noise computed by PSPICE and our FDTD model (90nm technology)

Rise Time (Ps)	90nm tech Vnoise/Vdd(%)	90nm tech Vnoise/Vdd(%)	
	FDTD	PSPICE	%Error
40	19,41	20,16	3,86
50	15,85	17,08	7,76
60	13,58	14,5	6,77
70	12,2	12,7	4,1
80	10,4	11,16	7,30
90	9,3	10,4	11,82
100	8,75	9,33	6,62
110	8,18	8,75	6,96
120	7,56	8	5,82
% Average error			6,77

Note that from Table 2 and Table 3, the FDTD method results in an average error of 4.14% and 6.77% as compared to PSPICE for 65 and 90 nanometer technologies generations respectively. It is to be noted that the peak crosstalk noise increases with the decreasing rise time of the input. In fact with decreasing rise time value of the input, the inductive effect becomes strong, so, the voltage peak increases.

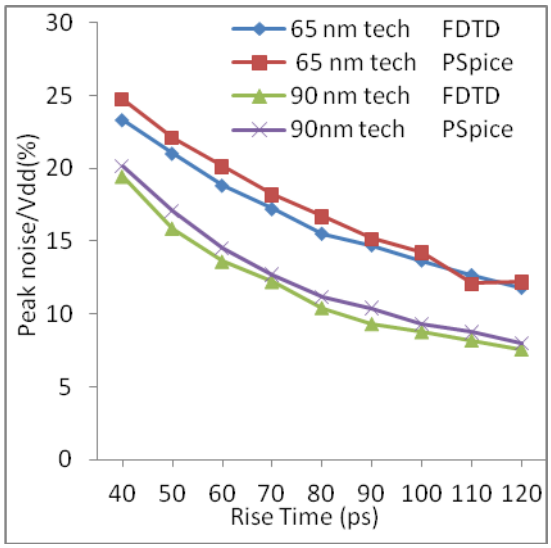

Figure 7 : Impact of rise time on peak crosstalk noise.

B. Impact of rise time on the propagation delay

To analyze the effects using the proposed algorithm FDTD computations and PSPICE simulations are carried out to determine propagation delay as a function of rise time. The FDTD computed and PSPICE simulation results are presented in figure 8.

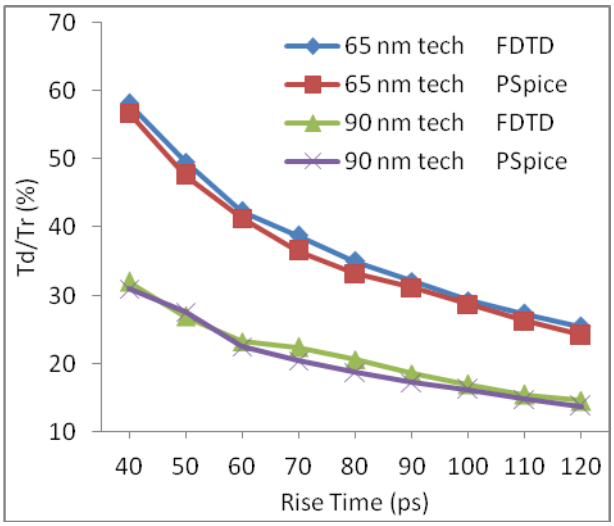

Figure 8 : Propagation delay as a function of rise time

The average error of the propagation delay as compared with PSPICE is 3.82% and 5.13% for 90nm and 65nm deep submicron technologies generations respectively. Notice that as the rise time of the input decreases the delay also decreases because the active transistor is not turned all the way on at once.

Conclusion

Understanding and predicting interconnect behavior is vital for designing high-performance integrated circuits. In this paper, we have presented an accurate closer form expression for the crosstalk amplitude between RLC coupled interconnects using FDTD method. It has summarized the coupling noise and line delay estimation for interconnects which have been useful to guide performance optimization in VLSI layout under the deep submicron technology. By comparing our FDTD results and PSPICE simulations, we have demonstrated the good accuracy of the proposed model. This work is integrated in problems aiming at bringing to designers fast and reliable solutions guaranteeing the signal integrity in the integrated systems.

References

[1] A. Vittal, L. H. Chen, M. Marek-Sadowska, K. P. Wang, S. Yang, “Crosstalk in VLSI Interconnections”, IEEE Trans. Computer-Aided Design, vol. 18, no. 12, pp. 1817-1824, 1999.

[2] K. Rahmat and O. S. Nakagawa and S-Y. Oh and J. Moll, "A Scaling Scheme for Interconnect in Deep-Submicron Processes", IEEE International Electron Devices Meeting, pp. 245-248, 1995.

[3] H. Belahrach, "Caractérisation électrique des interconnexions en technologie hybride : modélisation numérique et simulation temporelle", Ph.D of Bordeaux1 University, 1990.

[4] M. Satar, H. Belahrach, "On-Chip Coupling Noise Estimation Between Parallel Wires", Proc. ICONIC, pp. 159-163, Rouen, France, june 2003.

[5] Afrooz K., A. Abdipour, et al., "Time domain analysis of active transmission line using FDTD technique", Progress In Electromagnetics Research, vol. 77, pp. 309-328, 2007.

[6] Susmita Sahoo, Madhumanti Datta, et al., "FDTD based transition time dependent crosstalk analysis for coupled RLC interconnects", Journal of Semiconductors Vol.35, No.5, May 2014.

[7] Li X C, Mao J F, Swaminathan M., "Transient analysis of CMOS gate driven RLCG interconnects based on FDTD," IEEE Trans Computer-Aided Design of Inte-

grated Circuits and Systems, vol. 30 no. 4, pp. 574-583, 2011.
[8] BRANČÍK L., "Time-domain analysis of multiconductor transmission lines per implicit Wendroff method", Proc. of Int. IMAPS EDS 2010 Conference. Brno, pp. 45 – 50, 2010.
[9] Predictive Technology Model (PTM) Nanoscale Integration and Modeling Group, 2014.
[10] Susmita Sahoo, Madhumanti Datta, and Rajib Kar, "Explicit Delay and Power Estimation Method for CMOS Inverter Driving on-Chip RLC Interconnect Load", International Journal of Electrical and Electronics Engineering, pp.165-172, 2011.
[11] Sharma D. K., Mittal S., Kaushik B. K., et al., "Dy namic crosstalk analysis in RLC modeled interconnects using FDTD method", IEEE Intl. Conf. Computer and Communication Technology (ICCCT), pp. 326-330, 2012.

Biographies

MOULOUD SATAR received the M.S. degree in Electrical Engineering from the University of V.M.E.I, Sofia, Bulgaria, in 1988, and the University Accreditation in Microelectronics and communication from the University of Cady Ayyad, Marrakech, Morocco, in 2006. Currently he is an Professor of Electronic Digital, Microcontrollers and DSP at Royal Air Academy (Marrakech). His research areas include Noise Analysis and Design in Deep Submicron. His email-id is satarm2002@yahoo.fr

HASSAN BELAHRACH received the B.S. degree in Electrical and Electronics from the University of Mohamed V, Rabat, Morocco, in 1986, the M.S. degree in Electronics and Microelectrincs from the University of Bordeaux I, Bordeaux, France, in 1987, the Ph.D. degree in Microelectronics and technology from the University of Bordeaux I, Bordeaux, France, in 1990, and the Ph.D. degree in Microelectronics and Telecommunication from the University of Cady Ayyad, Marrakech, Morocco, in 2001, respectively. Currently, He is an Professor of Electronic Analog and Digital at Royal Air Academy (Marrakech). His research areas include Noise Analysis and Design in Deep Submicron. His email-id is h.belahrach@gmail.com.

ABDELILAH GHAMMAZ received the Doctor of Electronic degree from the National Polytechnic Institute (ENSEEIHT) of Toulouse, France, in 1993. In 1994 he went back to University Cadi Ayyad of Marrakech – Morocco. Since 2003, he has been a Professor at the Faculty of Sciences and Technology, Marrakech, Morocco. He is currently the vice-director of the Electrical Systems and Telecommunications Laboratory at Cadi Ayyad University of Marrakech, Morocco. His research interests concern electromagnetic compatibility and antennas. His email - id is aghammaz@yahoo.fr.