DESIGN AND ANALYSIS OF 48 BIT HETEROGENEOUS ADDER

Abstract

Adder is the important component of digital system. With increasing technology to depth, the speed of the circuit increases rapidly. But at the same time, the power consumption per chip is also increasing due to the wide density of the chip. Therefore, in realizing Very Large Scale Integration (VLSI) circuits, high speed and low power are the two predominant factors which need to be considered. In today’s world, where demand for portable battery operated devices is increasing, a major trust is given towards low power methodologies for high speed applications. In this paper there is try to determine the best solution to this problem by comparing a few adders.

In this paper when we compare the power consumption and delay of three different adders that is carry Select Adder, Carry Bypass Adder and Carry Look-ahead Adder using 90 nm and 180 nm technology. Then we design 16 bit Carry Select Adder, Carry bypass adder, carry look-ahead adder. With the help of these three adders 16 bit Carry select adder, 16 bit Carry bypass adder, 16 bit Carry look-ahead adder, a 48 bit heterogeneous adder is designed; we designed a heterogeneous adder to control power and delay of adder. For this 90 nm and 180 nm technology is used and 0.9 V, 1.8 V is used in these technologies respectively. Gate width is different and length used is 0.09μm and 0.18 μm. We use TANNER tool. The proposed adder has advantage of more speed and lesser power consumption.

Introduction

As we know, adder is the important component of digital system. So its power consumption, area and delay are of utmost importance. With rising technology, speed of circuits is increasing but on the other hand, power consumption per chip is also increasing. But in moderate improvement in performance of battery indicates that power consumption is important parameter and it should be less. With demand of probability and mobility, area per chip is also increasing. Hence three most important parameters are area, delay and power consumption.

To design a low power and high speed circuits can be addressed at various levels like as algorithm, layout, architecture, process technology and circuit levels. Nowadays, interest has been seen in the problems of designing of digital systems.

There are two types of power that is
1. Static power consumption
2. Dynamic power consumption

Static power consumption is that which mainly affect a system at rest.
\[ P_s = I_{\text{leakage}} \times V_{dd} \]

On contrast, dynamic power consumption is that which affects a system in active mode.

Dynamic power is attributed by two causes
1. Load capacitance charging/discharging
2. Short circuit

\[ P_{\text{total}} = P_{\text{switching}} + P_{\text{short-circuit}} + P_{\text{leakage}} \]
\[ = (\alpha_{0\rightarrow1} \times C_L \times V_{dd}^2 \times f_{clk}) + (I_{leakage} \times V_{dd}) \]

The first term represents the power consumption by capacitance charging discharging during circuit switching. Where C is load capacitance, \( \alpha_{0\rightarrow1} \) is node transition, \( f_{clk} \) is clock frequency. The second term is the power consume due to direct path between power supply and ground. The third term represents static power, when circuit at rest, basically static power is zero but due to leakage current, there is little bit static power. Thus voltage supply is the effective way to reduce the three types of power. Such a reduction requires new design methods for low-voltage and low power integrated circuits.

This paper is organized as follows. In section I, there are introduction. In Section II, we will review the different design styles. Section III describes the performance parameters of 1 bit different adders. In Section IV, about the 48 bit heterogeneous adder. In section V, Final result is shown and in section VI, conclusions are summarized.

II. Design styles

Adder is the commonly used block of digital signal processing and central processing unit. Its power optimization and delay is utmost importance. For arithmetic applications, following three different logic styles are used for a full adder design to gain best performance results

Carry Select Adder

In the figure 1 the full adder is built by 30 transistors by using TG technology. In this circuit, all simulations are run
using 90nm and 180 nm technology with different NMOS and PMOS width and 0.09um and 0.18 um length, a 0.9 V and 1.8 V power supply is used in 90nm and 180nm technology respectively. With the help of below 1bit CSA, 16-bit CSA is developed. In the circuit there are three inputs A, B and C and two outputs sum and carry.

**Fig 1: Carry Select adder using TG technology**

**B Carry look-ahead adder**

In the figure 2 the full adder is built by 30 transistors by using TG technology. In this circuit the design process all simulations are run using 90nm and 180 nm technology with different NMOS and PMOS width and 0.09um and 0.18 um length, a 0.9 V and 1.8 V power supply is used in 90nm and 180nm technology respectively. With the help of below 1bit CLA, 16-bit CLA is developed. In the circuit there are three inputs A, B and C and two outputs sum and carry.

**Fig 2: Carry Look-ahead Adder using TG technology**

**C Carry Bypass Adder**

In the figure 3, the full adder is built by 30 transistors by using TG technology. In this circuit the design process all simulations are run using 90nm and 180 nm technology with different NMOS and PMOS width and 0.09um and 0.18 um length, a 0.9 V and 1.8 V power supply is used in 90nm and 180nm technology respectively. With the help of below 1bit CBA, 16-bit CBA is developed. In the circuit there are three inputs A, B and C and two outputs sum and carry.

**Fig 3: Carry Bypass Adder TG technology**

**III Performance parameters of 1-bit different adder**

**A. Waveform of 1-bit Carry Select Adder**

Figure shows the waveform of 1-bit CSA. In this there are three inputs A, B and C and two outputs sum and carry.

**Waveform of 1bit CSA**
B. Waveforms of 1-bit carry look-ahead adder

Figure shows the waveform of 1 bit carry look-ahead adder. In this there are three inputs A, B and C and two outputs sum and carry.

C. Waveforms of 1bit carry bypass adder

Figure shows the waveform of 1-bit carry bypass adder. In this there are three inputs A, B and C and two outputs sum and carry.

IV. 48 bit heterogeneous adder

Firstly, We extend 1 bit CSA, CBA, CLA into 16 bits. Then with the help of 16 bit CSA, 16 bit CBA, 16 bit CLA, we design a 48 bit heterogeneous adder, we choose different adders to design a 48 bit adder, so that we can control both power consumption and delay. Comparison is done using 90 nm technology and 180 nm technology.

V. Final result

Results of 48 bit heterogeneous adder using 90nm and 180nm technology are shown below.

<p>| Table 5.1 Performance parameters of 48 bit adder at 180 nm technology |
|---------------------------|---------------------------|---------------------------|---------------------------|</p>
<table>
<thead>
<tr>
<th>Design</th>
<th>Style</th>
<th>No. of transistors</th>
<th>Minimum Length (µm)</th>
<th>Avg. Power Consum. (mW)</th>
<th>Prop. Delay at carry (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heterogeneous Adder</td>
<td>1440</td>
<td>0.18</td>
<td>1.12</td>
<td>12.1</td>
<td></td>
</tr>
</tbody>
</table>

<p>| Table 5.2 Performance parameters of 48 bit adder at 90 nm technology |
|---------------------------|---------------------------|---------------------------|---------------------------|</p>
<table>
<thead>
<tr>
<th>Design</th>
<th>Style</th>
<th>No. of transistors</th>
<th>Minimum Length (µm)</th>
<th>Avg. Power Consum. (mW)</th>
<th>Prop. Delay at carry (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heterogeneous Adder</td>
<td>1440</td>
<td>0.09</td>
<td>0.09</td>
<td>24.1</td>
<td></td>
</tr>
</tbody>
</table>

Average power and delay are calculated using different PMOS and NMOS width and minimum length of 0.09um and 0.18 um.0.9 V power supplies is used in 90nm technology and 0.18 V is used on 180 nm technology.

VI. Discussion and conclusion

We have carried out a comparison among the most suitable topologies of 16-bit different adders. The comparison has been carried out both assuming circuits with minimum transistors size, to minimize the power consumption. By measuring the performance parameters of 48 bit heterogeneous adder, we conclude that power dissipation using 0.09 technology is less as compared to 0.18 technologies. But delay using 0.18um technology is less as compared to 0.09um technology.
REFERENCES


Biographies

VEERPAL KAUR received B.Tech degree in Electronics and Communication Engineering from Yadavindra College Of Engineering, Talwandi Sabo, City Bathinda, State Punjab (India) in 2007-2011. Currently, She is pursuing Mtech part time from Yadavindra College Of Engineering and working as a lecturer in Gyan Sagar Polytechnic College, Baghapurana (Moga). Her research interests include VLSI circuit design. Er. Veerpal Kaur may be reached at bveerpal80@yahoo.com.

ASHWANI KUMAR was born in Punjab, INDIA. He has received his B.Tech from G.N.D.U Amritsar and M.Tech. from PTU, Jalandher. He has more than 15 years of experience of teaching and research. He has published Various papers in national and international journals. His main Research interests are VLSI & Mobile Adhoc Networks. Presently, he is pursuing Phd and working as Asst. Prof. in YCOE, Bathinda.